NEC microcomputers, inc.

μPD372

FLOPPY DISK CONTROLLER
USERS' MANUAL

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Rev/2

NEC MICROCOMPUTERS, INC.

uPD372D

LSI FLOPPY DISK CONTROLLER CHIP

USERS' MANUAL

March 11, 1977

The NEC uPD372D is a high performance N-channel LSI floppy disk controller designed to interface between most minicomputers or microprocessors and most floppy disk drives.

The uPD372D is the most versatile floppy disk controller chip available.

FEATURES
- Compatible with IBM3740 format
- Compatible with Shugart Minifloppy format
- Compatible with many other formats
- Generates and checks Cyclic Redundancy Characters
- Initiates operations at address marks or physical index
- Formats clear disks
- Handles up to four floppy disk drives
- Can read or write on one drive while simultaneously track seeking on another
- Track stepping rate and step pulse width are programmable
- Sector size programmable from one byte to one sector per track
- Data transfer rate easily changed
- Standard power supply voltages +12V, +5V, -5V

The uPD372D is compatible with most floppy disk drives including:

Calcomp 140	Pertec FD400
CDC BR803	Potter DD4740
GSI 050	Remex RFS7400
GSI 110	Shugart SA400
Innovex 210	Shugart SA900
Orbis 74	Sycor 145
Persci 75	

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INTRODUCTION

The uPD372 may be interfaced directly to a host processor as shown in Figure 1 or it may be interfaced to a controller processor which in turn is interfaced to the host processor as shown in Figure 2. Most processors interfaced to the uPD372 must, when reading from or writing a record on the disk, be completely dedicated to the task of controlling the disk drive(s). These periods may last several milliseconds. If the nature of the other tasks performed by the host processor allows them to be neglected for this length of time, then the uPD372 may be interfaced directly to the host processor. Otherwise, a controller processor is required.

Whichever approach is chosen, the floppy disk drive control workload is shared between the uPD372 hardware and the processor(s) software.

The uPD372 converts information, which the software

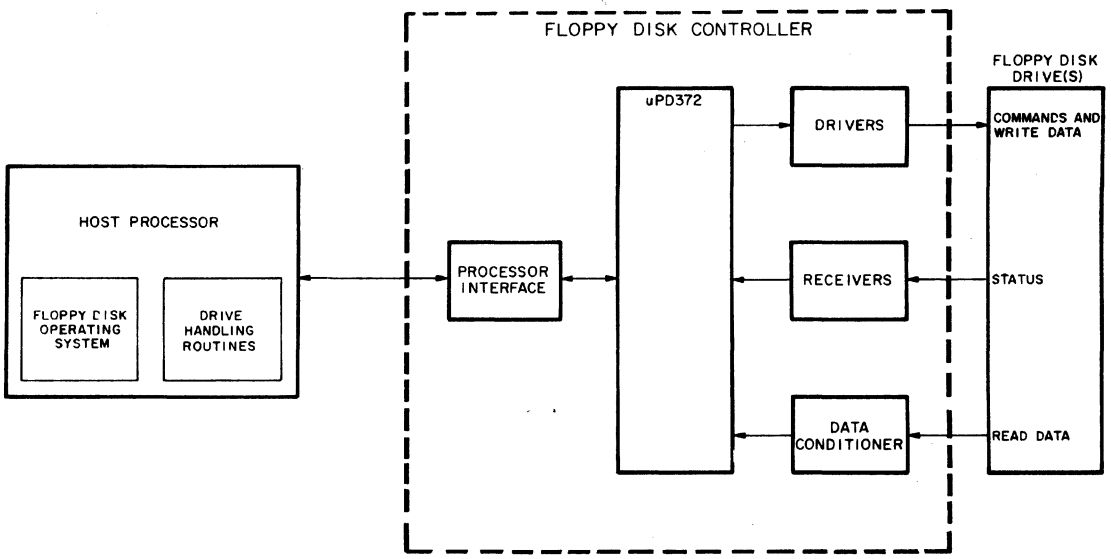


FIGURE 1
uPD372 INTERFACED DIRECTLY TO HOST PROCESSOR (15-20 CHIPS)

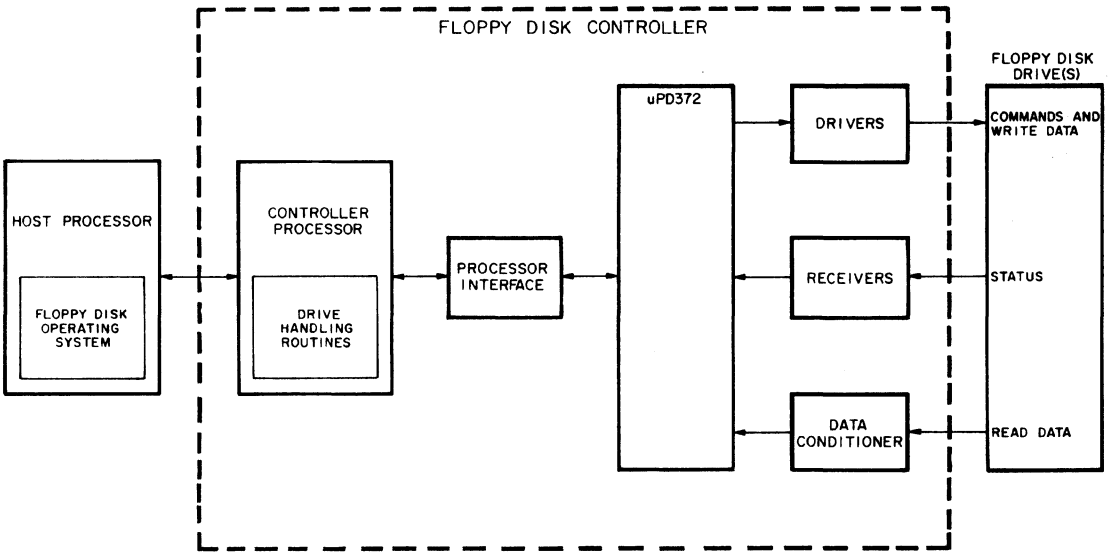


FIGURE 2
uPD372 INTERFACED TO HOST PROCESSOR THROUGH CONTROLLER PROCESSOR (34-40 CHIPS)

INPUT/OUTPUT SIGNALS

INTRODUCTION

Figure 3 shows the input/output signals of the uPD372 grouped into 10 categories.

RESET
REGISTER SELECT COMMANDS
INTERRUPT REQUEST
DATA BUS
TIMING
WRITE DATA
DISK DRIVE COMMANDS
READ DATA
DISK DRIVE STATUS
MISCELLANEOUS

The REGISTER SELECT COMMANDS control Data Transfers from the DATA BUS to the 6 uPD372 write registers. The contents of the write registers are translated by the uPD372 into WRITE DATA and DISK DRIVE COMMANDS. The REGISTER SELECT COMMANDS also control Data Transfers from the 3 uPD372 read registers to the data bus. The processor may then read the DISK DRIVE STATUS and READ DATA from the data bus.

The processor generates DISK DRIVE COMMANDS by manipulating bits in the uPD372 write registers and the DISK DRIVE STATUS signals control the state of bits in the read registers. To avoid repetition the signals in these two categories are described in the ADDRESSABLE INTERNAL REGISTERS section only. All other input/output signals are described below.

Processor Interface

Reset

Pin 1 RST (Reset)

A logic one at pin 1 causes a general reset of the uPD372. For a list of signals and registers affected, see RST-bit 7 of Write Register 0 (WR0) in the ADDRESSABLE INTERNAL REGISTERS section.

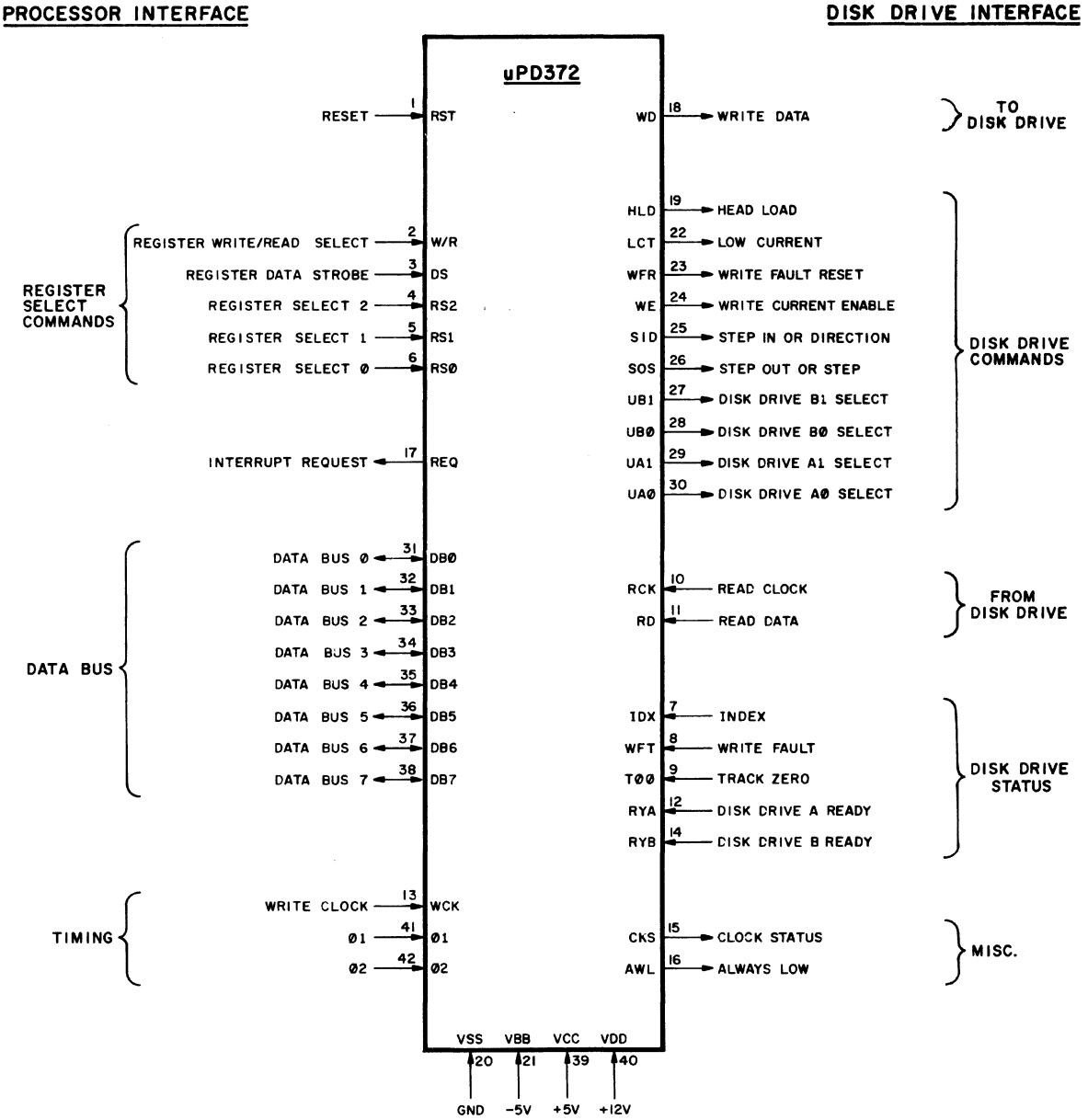


FIGURE 3
INPUT/OUTPUT SIGNALS

Register Select Commands and Data Bus

Pin 2	W/R	(Register Write/Read Select)
Pin 3	DS	(Register Data Strobe)
Pins 4-6	RSØ-RS2	(Register Address)
Pins 31-38	DBØ-DB7	(Data Bus)

W/R, DS and RSØ-RS2 control Data Bus transfers between the uPD372 and the processor as follows:

Writing into a uPD372 register

When W/R is a logic one, information the processor places on DBØ-DB7 is written into the uPD372 Write Register selected by RSØ-RS2. The information is written at the time of the trailing edge of each Ø2 which occurs while DS is a logic one.

Reading from a uPD372 register

When W/R is a logic zero, information from the uPD372 Read Register selected by RSØ-RS2 is placed on DBØ-DB7 to be read by the processor. The information remains on DBØ-DB7 as long as DS is a logic one. See uPD372 SIGNAL TIMING DIAGRAM, Figure 12 for exact timing.

NOTE: The logic condition which places uPD372 READ Register information on the Data Bus is $DS \cdot \overline{W/R} \cdot \overline{RS2}$. If these three signals are allowed to change asynchronously with respect to each other, care must be taken to insure that this condition does not become true inadvertantly. The simplest method is to require that W/R and RS2 must not change state while DS is a logic one.

NOTE: RSØ and RS1 must not change state during the period from 15Øns before until 1Øns after the trailing edge of Ø1 or else register contents and DISK DRIVE COMMANDS may be modified. A simple method to accomplish this is to use a dual flip-flop to synchronize changes in RSØ and RS1 with the leading edge of Ø2(TTL) as shown in Figure 1Ø.

Interrupt Request

Pin 17 REQ (Interrupt Request)

Interrupt requests are generated by the uPD372 only while STT (Start-bit 5 of WR3) is true. Two types of interrupt requests occur -- Index Requests and Data Requests.

Index Requests occur once per disk revolution when the physical index hole passes a photodetector. See IRQ-bit 1 of Read Register Ø (RRØ) in the ADDRESSABLE INTERNAL REGISTERS section.

Data Requests begin during disk reading after an address mark is read and then occur each time an eight-bit byte, assembled from disk serial data, is available to be read by the processor program. Data requests occur during disk writing or formatting each time an eight-bit byte is required from the processor program. See DRQ-bit Ø of Read Register Ø (RRØ) in the ADDRESSABLE INTERNAL REGISTERS section.

Timing Signals

Pin 41 Ø1

Pin 42 Ø2

The uPD372 requires two MOS level clock signals, Ø1 and Ø2. A uPD8224 generates both Ø1 and Ø2 as well as a TTL level Ø2. If the uPD372 is interfaced to a uPD8Ø8ØA microprocessor and if both devices are in the same proximity, they may share a uPD8224 as shown in Figure 1Ø.

Pin 13 WCK (Write Clock)

WCK determines the bit transfer rate to the selected disk drive while writing. IBM standard drives require a 5ØØKHz WCK. The Shugart Minifloppy requires a 25ØKHz WCK. Other standards may require different WCK frequencies. In each case the WCK frequency should be twice the bit transfer rate.

DISK DRIVE INTERFACE

Write Data

Pin 18 WD (Write Data)

Serial Frequency Modulated (FM) code to be written on a floppy disk leaves the uPD372 at pin 18. Pin 18 should be connected to the WRITE DATA input of the selected disk drive.

Disk Drive Commands

The following commands to the disk drive(s) are generated under program control by modifying the contents of uPD372 Write Registers. The description of each command may be found in the ADDRESSABLE INTERNAL REGISTERS section under the appropriate write register and register bit.

Pin 19	HLD (Head Load)	See Write Register Ø (WRØ) bit 3
Pin 22	LCT (Low Current)	See WRØ bit 2
Pin 23	WFR (Write Fault Reset)	See WRØ bit 1
Pin 24	WE (Write Current Enable)	See WR3 bits 2 and 4
Pin 25	SOS (Step Out or Step)	See WR4 bit 5
Pin 26	SID (Step In or Direction)	See WR4 bit 6
Pin 27	UB1 (Disk Drive B1 Select)	See WR4 bit 1
Pin 28	UBØ (Disk Drive BØ Select)	See WR4 bit Ø
Pin 29	UA1 (Disk Drive A1 Select)	See WR1 bit 1
Pin 3Ø	UAØ (Disk Drive AØ Select)	See WR1 bit Ø

Read Data

Pin 1Ø RCK (Read Clock)

Pin 11 RD (Read Data)

RD is a changing logic level updated by each data and clock pulse in the raw data read from the selected disk drive. RCK is a clock the positive transition of which strobes RD into the uPD372. Both signals are derived from the raw data by the DATA CONDITIONER circuit. See the DATA CONDITIONER section for a complete description of RCK and RD.

Disk Drive Status Signals

The following status signals from the disk drive(s) each control the logic level of a bit in uPD372 Read Registers Ø and 1 (RRØ and RR1). By reading the contents of these registers the processor program senses the disk drive status signals. A description of each status signal may be found in the ADDRESSABLE INTERNAL REGISTERS section under the appropriate read register and bit.

Pin 7	IDX (Index)	See Read Register Ø (RRØ) bit 1
Pin 8	WFT (Write Fault)	See RR1 bit 2
Pin 9	TØØ (Track Zero)	See RR1 bit 6
Pin 12	RYA (Disk Drive A Ready)	See RR1 bit 3
Pin 14	RYB (Disk Drive B Ready)	See RRØ bit 6

Miscellaneous

Pin 15 CKS (Clock Status)

A logic one at CKS indicates that the uPD372 has been commanded (by WCS, bit 6-WR3) to operate with timing signals from the Write Clock (WCK, pin 13). A logic zero at CKS indicates that the uPD372 has been commanded (by RCS, bit 7-WR3) to operate with timing signals from the Read Clock (RCK, pin 1Ø).

Pin 16 AWL (Always Low)

AWL is a logic zero output under all normal operating conditions.

ADDRESSABLE INTERNAL REGISTERS

INTRODUCTION

Data transfers to and from the uPD372 addressable internal registers are controlled by signals W/R, DS and RSØ-RS2 at pins 2-6. These signals are discussed in the INPUT/OUTPUT SIGNALS section.

The address of each register and a mnemonic abbreviation for each register bit are shown in Figure 4. The function initiated, controlled or signalled by each register bit is described in this section.

An important internal timing signal, the Bit Ring Pulse (BRP), affects the functions of more than one third of the register bits. The BRP is a pulse that occurs each time 8-bits (one byte) of data have been read from or written on the disk.

While reading:

the first BRP occurs when the first I.D. address mark, Data address mark or Deleted Data address mark is read after STT (bit 5 of WR3) has been set. BRP's continue to occur each time 8 bits (1 byte) have been read until STT is reset.

While writing:

BRP's occur each time 8 bits (1 byte) have been written until STT is reset.

While formating:

the first BRP occurs when the physical index hole passes the floppy disk drive photodetector after IXS and STT (bits 3 and 5 of WR3) have been set. BRP's continue to occur each time 8 bits (1 byte) have been written until STT is reset.

REGISTER ADDRESS				REGISTER NAME	BIT NUMBERS							
W/R	RS2	RS1	RS0		7	6	5	4	3	2	1	0
WRITE REGISTERS												
1	0	0	0	WR0	RST	MBL	X	X	HLD	LCT	WFR	X
1	0	0	1	WR1	CBS	X	CB5	CB4	CB3	UAS	UA1	UA0
1	0	1	0	WR2	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
1	0	1	1	WR3	RCS	WCS	STT	WES	IXS	WER	CCG	CCW
1	1	0	0	WR4	STS	SID	SOS	X	X	UBS	UB1	UB0
1	1	1	0	WR6	X	X	X	X	X	TRR	IRR	DRR
READ REGISTERS												
0	0	0	0	RR0	ALH	RYB	UB1	UB0	ERR	TRQ	IRQ	DRQ
0	0	0	1	RR1	WRT	T00	DER	COR	RYA	WFT	UA1	UA0
0	0	1	0	RR2	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

X=NOT USED

FIGURE 4
ADDRESSABLE INTERNAL REGISTERS

WRITE REGISTERS

Write Register 0 (WR0)

WR0-Bit 0 Not Used.

WR0-Bit 1 WFR (Write Fault Reset)

A logic one transmitted to bit 1 sets the output of WFR pin 23 to a logic one. The one logic level remains at pin 23 until a logic zero is transmitted to bit 1. The signal at pin 23 may be used for any command purpose, but normally is used to reset a Write Fault condition.

To reset Write Fault, a logic one is transmitted to bit 1 and about 10us later a logic zero is transmitted to bit 1. This forms an approximately 10us wide pulse at pin 23 - the width specified by most disk drive manufacturers.

A Write Fault is signaled by a drive whenever an attempt is made to turn on the write current illegally (viz. when the head is not loaded). The Write Fault condition is sensed by the processor in bit 2 of RR1.

The status of ICT and HIP, bits 2 and 3 of WR0 should be

A logic one at the HLD bit sets the Head Load flip-flop. A logic zero resets the flip-flop. The Q output of the Head Load flip-flop is internally connected to pin 19, HLD. Pin 19 should be connected to the floppy disk drive HEAD LOAD input control line.

The head requires a settling time (approx. 40ms -- see drive specifications) after loading the head and before reading or writing begins.

The state of LCT, bit 2, WRØ should be preserved during Head Load commands. See the note after bit 7 of WRØ.

WRØ-Bit 4 Not Used.

WRØ-Bit 5 Not used.

WRØ-Bit 6 MBL (Must Be Low)

This bit must be a logic zero during each command to WRØ.

WRØ-Bit 7 RST (Reset)

A logic one transmitted to bit 7 resets the uPD372. The effect is exactly the same as that of a pulse on pin 1.

All bits in all write registers; all bits in the read data register, RR2; all disk drive command signals; and Write Data (pin 18) are set to a logic zero.

NOTE: Commands are made to individual bits in WRØ. However, every WRØ bit is affected by any data transfer to WRØ. For instance, to load the head of the selected drive, HLD is set to a one, but what should the other bits of the command be? RST, MBL and WFR should be zero. Bits Ø, 4 and 5 may be anything but the LCT status of the selected drive should be left unchanged. Consequently, a software image of HLD and LCT must be maintained for each drive. Whenever HLD, LCT or WFR is addressed, the selected drive HLD and LCT status must be recalled and incorporated in the command data transfer. This is accomplished by the WRØ MANAGER subroutine in the software listing for the FLOPPY DISK CONTROLLER EXAMPLE given in this manual.

Write Register 1 (WR1)

WR1-Bit Ø UAØ (Unit AØ Set)

WR1-Bit 1 UA1 (Unit A1 Set)

WR1-Bit 2 UAS (Unit A Strobe)

Bit 0 (UA0) and bit 1 (UA1) control the logic levels of output pins 30 (UA0) and 29 (UA1) respectively. These logic levels may be used for any command function. The logic levels at pins 30 and 29, along with these at pins 28 and 27 (see WR4 bits 0, 1 and 2 -- UB0, UB1 and UB5) could simply be the select signals for four disk drives. Or, in a more sophisticated system, UA0 and UA1 can select one of up to four drives for a read or write operation and UB0 and UB1 can select another of the drives for a simultaneous track seek operation.

If bit 2, UAS is a logic zero when addressing WR1, the logic levels at pins 30 and 29 remain unchanged regardless of the content of bits 0 and 1. If bit 2 is a logic one when addressing WR1, the logic levels at pins 30 and 29 are set to the logic levels of bits 0 and 1. This allows the write clock bits (bits 3, 4, 5 and 7 of WR1) to be addressed independently from the Unit A select bits.

WR1-Bit 3 CB3 (Write Clock Bit 3)

WR1-Bit 4 CB4 (Write Clock Bit 4)

WR1-Bit 5 CB5 (Write Clock Bit 5)

WR1-Bit 6 (Not Used)

WR1-Bit 7 CBS (Write Clock Bit Strobe)

IBM specifications include definitions of four special byte code patterns termed "address marks". See the INTRODUCTION of the DATA CONDITIONER section for a discussion of code patterns and address marks. What distinguishes the address marks from other bytes sent to or read from the disk is that some of the "clock" pulses are missing.

The clock pattern for ID address marks, Data address marks and Deleted Data address marks is a C7 (hex). The clock pattern for the Index address mark is D7 (hex). Since all clock pulses are present for every other byte (gap or data byte) the clock pattern is FF (hex).

For all three clock patterns bits 0, 1, 2, 6 and 7 must be logic ones. Only bits 3, 4 and 5 may be zeros. During writing the uPD372 allows the state of clock bits 3, 4 and 5 to be

controlled by CB3, CB4 and CB5. The other clock bits are always logic ones.

In order to change the state of CB3, CB4 or CB5, CBS must be a logic one. If CBS is a zero, CB3, CB4 and CB5 are unaffected by data transfers into WR1.

To set an FF (hex) clock pattern for data and gap bytes, B8 (hex) should be written into WR1. To set a C7 (hex) clock pattern for ID, Data or Deleted Data address marks, 80 (hex) should be written into WR1. To set a D7 (hex) clock pattern for Index address marks, 90 (hex) should be written into WR1.

Write Register 2 (WR2)

WR2-Bits 0-7 WD0-WD7 (Write Data Register)

When the uPD372 is writing on the disk, the data from WR2 and the clock pattern from WR1 are transferred to a 16-bit shift register once every 16 Write Clock (WCK) cycles. The data and clock bits are frequency modulation encoded and serially transmitted from the shift register through pin 18, WD (Write Data) to the selected floppy disk drive read/write head.

If the processor does not transfer new data to WR2, the write data pattern in WR2 remains constant and is repeatedly written on the disk.

Write Register 3 (WR3)

WR3-Bit 0 CCW (Cyclic Check Words)

CCW must be set to a one while the floppy disk drive read/write head is either reading or writing the last data byte of an ID or data record. It must be reset to a zero while the head is reading or writing the second CRC byte. See program listings for READ ID, READ DATA and WRITE DATA for exact sequence.

In the Read Mode, the Bit Ring Pulse (BRP) which follows the setting of CCW begins a bit-by-bit serial comparison between the CRC bytes read from the disk and the CRC bytes generated and stored in the uPD372 CRC register. The comparison ends at the time of the BRP which follows the resetting of CCW. The same BRP sets bit 5 of RR1 (DER-Data Error) to a one if an error was detected. DER is set to a zero if no error was detected. The DER information remains valid for one byte time (while the head is reading the first gap byte following the record).

In the Write mode, CCW is used to write the two CRC bytes. The BRP which follows the setting of CCW causes write data to be

taken from the CRC register rather than the write data register, WR2. The writing of the CRC bytes ends at the time of the BRP following the resetting of CCW. See program listing for WRITE DATA.

WR3-Bit 1 CCG (Write Cyclic Check Generator Start)

CCG is used only in the write mode to start the calculation of the CRC. (CRC calculation begins automatically at the address mark in the read mode.) CCG must be set to a one while the head is writing the last gap byte before writing an ID or Data record. CRC calculation begins at the time of any BRP which occurs while CCG is a one. Consequently, CCG must be reset to a zero while the head is writing the first byte (address mark) of the record

Writing:

Each write operation is preceded by a READ ID routine (which STT starts). STT remains a logic one during READ ID, during the gap between the ID record and the data record and while writing a new data record. STT is not reset until the data record has been written.

The clock source is switched to the Write Clock and write current is enabled 11 bytes (in IBM format) after the ID record. Writing begins at the next BRP. Six new gap bytes are written, the data record is written and one new byte in the following gap is written before STT is reset. After STT is reset, the next (and last) BRP resets the write current.

BRP's and interrupt requests occur at each byte from the start of READ ID until STT is reset at the end of WRITE DATA. See listing of WRITE DATA.

Formatting:

A 78 (hex) is transmitted to WR3 (STT, WCS, WES and IXS = 1). The next physical index signal (IDS pin 7) enables the write current and starts a series of BRP's and interrupt requests. These continue for one entire disk revolution while the track is being formatted with data bytes, gap bytes and address marks provided by the processor. STT is reset at the next index request flag (IRQ bit 1 of RRØ) ending the BRP's and interrupt requests and turning off the write current. See the listing of the FORMAT routine.

Resetting STT automatically resets Write Enable, sets WCS (Write Clock Set) and prevents further data requests (DRQ) and index requests (IRQ). See program listings of READ ID, READ DATA and WRITE DATA for examples of the use of STT.

WR3-Bit 6 WCS (Write Clock Set)

WR3-Bit 7 RCS (Read Clock Set)

WCS and RCS do not enable write current nor do they determine whether the uPD372 is in the write mode or the read mode; they simply select one of two sources of clock signals for the internal timing of the uPD372. The two clock sources are WCK (Write Clock-pin 13) and RCK (Read Clock-pin 1Ø). Both signals have a frequency of 5ØØKHz (2usec period) for IBM format. WCK should be derived from a crystal controlled oscillator. RCK must be derived from and synchronized with data and clock pulses read from a disk. This is accomplished by the DATA CONDITIONER circuit. See DATA CONDITIONER section.

The Read Clock is used only when STT is set and data is being read from the disk. The Write Clock is the normal clock source. The timing source is switched from the Read Clock to the Write Clock by any of the following.

1. By the BRP following the setting of WCS.

2. By resetting STT

3. By RST

The logic level of CKS (Clock Status) pin 15 is set high by any of the above.

The source of timing signals is switched from WCK to RCK by setting RCS. The logic level of CKS is set low by RCS.

Write Register 4 (WR4)

WR4-Bit 0 UB0 (Unit B0 Select)

WR4-Bit 1 UB1 (Unit B1 Select)

WR4-Bit 2 UBS (Unit B Strobe)

Bit 0 (UB0) and bit 1 (UB1) control the logic levels of output pins 28 (UB0) and 27 (UB1) respectively. These logic levels may be used for any command function. The logic levels at pins 28 and 27, along with those at pins 30 and 29 (see WR1 bits 0, 1 and 2--UA0, UA1 and UAS) could simply be the select signals for four disk drives. Or, in a more sophisticated system, UA0 and UA1 can select one of up to four drives for a read or write operation and UB0 and UB1 can select another of the drives for a simultaneous track seek operation.

If bit 2, UBS is a logic zero when addressing WR4, the logic levels at pins 28 and 27 remain unchanged regardless of the content of bits 0 and 1. If bit 2 is a logic one when addressing WR4, the logic levels at pins 28 and 27 are set to the logic levels of bits 0 and 1. This allows the step bits (bits 5, 6 and 7 of WR4) to be addressed independently from the unit B select bits.

WR4-Bit 3 Not used

WR4-Bit 4 Not used

WR4-Bit 5 SOS (Step Out or Step)

WR4-Bit 6 SID (Step In or Direction)

WR4-Bit 7 STS (Step Strobe)

Bits 5 (SOS) and 6 (SID) control the logic levels of output pins 26 (SOS) and 25 (SID) respectively. These logic levels may be used for any command function but are normally used to form stepping pulses to move the read/write head of the selected drive.

The step pulse width, repetition rate and the direction control scheme vary from one drive to another. The uPD372 can adapt to any drive with software changes only. For instance, many drives require a DIRECTION logic level to determine which direction (in or out) the read/write head is to move and a STEP pulse to trigger the actual movement. For these drives uPD372

WR6-Bit Ø DRR (Data Request Reset)

A logic one transmitted to DRR resets the Data Request, DRQ. See DRQ bit Ø of RRØ.

WR6-Bit 1 IRR (Index Request Reset)

A logic one transmitted to IRR resets the Index Request (IRQ). See IRQ bit 1 of RRØ.

WR6-Bit 2 TRR (Timer Request Reset)

A logic one transmitted to TRR resets the Timer Request (TRQ). See TRQ bit 2 of RRØ.

WR6-Bit 3-Bit 7 Not Used.

READ REGISTERS

Read Register Ø (RRØ)

RRØ-Bit Ø DRQ (Data Request)

When DRQ is true, the processor controlling the uPD372 should read a data byte from RR2 during the read mode or transmit a data byte to WR2 during the write mode.

DRQ causes an Interrupt Request (REQ) at pin 17.

DRQ's are generated as follows:

1. During the read mode the first ID address mark, Data address mark or Deleted Data address mark (but not Index address mark) which is read following the setting of STT (bit 5-WR3) sets DRQ. From this point on, DRQ is set again by every BRP (i.e., after every byte--data byte, gap byte or address mark--is read) until STT is reset. DRQ must be reset, by DRR (Data Request Reset--bit Ø, WR6) each time that it is set. If DRQ is still true at the time of the following BRP, a Command Overrun Error results (signaled by COR--bit 4, RR1). DRQ is automatically reset when STT is reset.

2. During the write mode Data Requests occur at each BRP (i.e., after each byte--data byte, gap byte or address mark--is written). As in (1) above, DRQ must be reset each time that it is set or a Command Overrun Error results.

3. During formatting a series of DRQ's begins when the physical index hole is detected after setting STT and IXS (bits 3 and 5 of WR3). The DRQ's continue to occur at every BRP until STT is reset. (STT and IXS should be reset at the end of one complete revolution--when IRQ, Index Request, bit 2, RR6 becomes true.)

RRØ-Bit 1 IRQ (Index Request)

IRQ is set true by the leading edge of the physical index pulse. The physical index pulse is generated when the index hole of the floppy disk passes a photo detector in the disk drive. STT must be set to enable IRQ.

IRQ causes an Interrupt Request (REQ--pin 17).

IRQ is reset by transmitting a logic one to IRR (Index Request Reset--bit 1, WR6), by resetting STT and by RST.

RRØ-Bit 2 TRQ (Timer Request)

TRQ is the Q output of a flip-flop which is set by every 512th Write Clock (WCK, pin 13) pulse. The Write Clock period for IBM compatible controllers is 2us causing TRQ to be set every 1.Ø24msec. TRQ is set every 2.Ø48msec when using Shugart Minifloppy format.

TRQ does not cause an Interrupt Request (REQ, pin 17).

TRQ is reset by transmitting a logic one to TRR (Timer Request Reset--bit 2, WR6) and by RST.

RRØ-Bit 3 ERR (Error)

ERR indicates a condition that must be corrected before issuing a command to the disk drive. ERR is the logical OR of three status signals:

$$ERR = WFT + \overline{RYA} + COR$$

where: WFT is Write Fault--bit 2, RR1

RYA is Disk Drive A Ready--bit 3, RR1

COR is Command Overrun--bit 4, RR1

$\overline{RYB}$ is not involved in the calculation of ERR.

RRØ-Bit 4 UBØ (Drive BØ Selected)

RRØ-Bit 5 UBl (Drive Bl Selected)

UBØ and UBl are two of the four status bits (the other being bits Ø and 1 of RRl) that indicate which disk drive has been selected. See descriptions of bits Ø, 1 and 2 of WR4 and pins 27 and 28.

RRØ-Bit 6 RYB (Drive B Ready)

This status bit indicates the logic level of RYB at pin 14. Pin 14 is usually connected to the READY output of the drive selected by UBØ and UBl (bits Ø and 1 of WR4).

RRØ-Bit 7 ALH (Always High)

This bit is a logic one as long as power is supplied to the uPD372.

Read Register 1 (RRl)

RRl-Bit Ø UAØ (Drive AØ Selected)

RRl-Bit 1 UAl (Drive Al Selected)

UAØ and UAl are two of the four status bits (the other being bits 4 and 5 of RRØ) that indicate which disk drive has been selected. See descriptions of bits Ø, 1 and 2 of WRl and pins 29 and 3Ø.

RRl-Bit 2 WFT (Write Fault)

This status bit indicates the logic level of WFT, pin 8. Pin 8 is usually connected to the WRITE FAULT output of the selected drive. A write fault condition occurs when a floppy disk drive detects an illegal command during a write operation. All commands to that drive are ignored as long as the write fault condition exists. The write fault is reset by WFR, bit 1, WRØ.

RRl-Bit 3 RYA (Drive A Ready)

This status bit indicates the logic level of RYA at input pin 12. Pin 12 is usually connected to the READY output of the drive selected by UAØ and UAl (bits Ø and 1 of WRl).

RR1-Bit 4 COR (Command Overrun)

COR indicates that the processor did not respond in time to a Data Request (DRQ) during either a read or a write operation. See DRQ, bit Ø of RRØ.

RR1-Bit 5 DER (Data Error)

DER indicates that a CRC error occurred during a read operation. DER is explained in detail in the description of CCW (Cyclic Check Words) bit Ø of WR3.

RR1-Bit 6 TØØ (Track Zero)

This status bit indicates the logic level of TØØ at input pin 9. Pin 9 is usually connected to the TRACK ØØ output of the selected disk drive. The disk drive places a high logic level on TRACK ØØ when and only when the read/write head is at track zero.

RR1-Bit 7 WRT (Write Mode)

WRT indicates which clock signals the uPD372 is using for internal timing--Write Clock (WCK, pin 13) or Read Clock (RCK, pin 1Ø). The selection is made by WCS (Write Clock Select) or RCS (Read Clock Select) bits 6 and 7 of WR3.

The logic level of WRT is identical to the logic level of CKS, output pin 15.

Read Register 2 (RR2)

RR2-Bits Ø-7 RDØ-RD7 (Read Data Register)

Data, serially read from the selected disk drive, is assembled into 8-bit parallel bytes in an internal shift register and is then transferred to RR2 at each BRP. See READ ID and READ RECORD routines for examples of the use of the Read Data Register.

DATA CONDITIONER

INTRODUCTION

Frequency modulation encoded data as transmitted to or received from a floppy disk drive consists of a series of timing or "clock" pulses interleaved with a series of data pulses (see Figure 5). The period between successive clock pulses is termed a "data cell". The presence of a data pulse within a data cell represents a logic one data bit. The absence of a data pulse within a data cell represents a logic zero data bit.

The clock pulses also contain information. Just as with the data pulses the presence of a clock pulse within a data cell represents a logic one clock bit. And, the absence of a clock pulse within a data cell represents a logic zero clock bit. Each byte is made up of eight data bits and eight clock bits for a total of sixteen.

Since the data read from a floppy disk is in serial format, the controller must have some means of distinguishing between clock bits and data bits and must also be able to determine the beginning of each byte. To provide this synchronization, soft-sectored floppy disks are written with a special byte, an

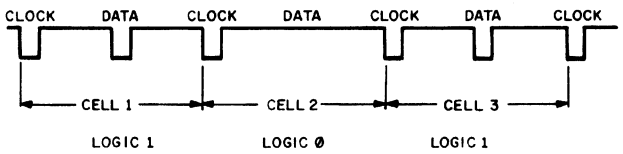


FIGURE 5
FLOPPY DISK DRIVE SERIAL DATA FORMAT

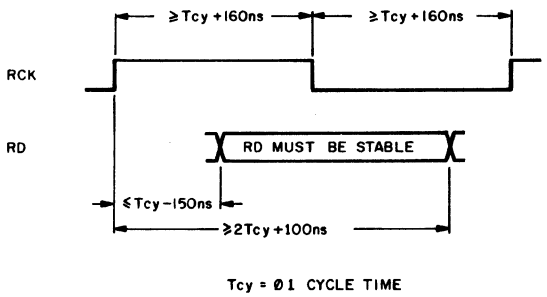


FIGURE 6
READ CLOCK (RCK) AND READ DATA (RD) REQUIRED BY uPD372

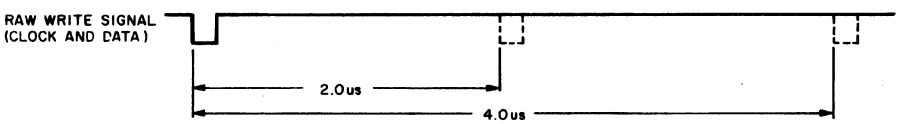


FIGURE 7
IBM FORMAT WRITE DATA TRANSMITTED TO DRIVE

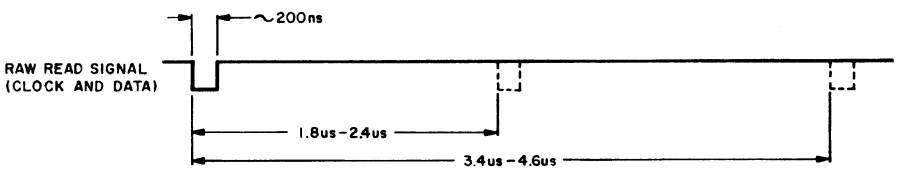


FIGURE 8
SAME DATA READ BACK (TRACK 76)

Each bit (clock and data) received by the uPD372 from a floppy disk drive is clocked into a sixteen bit shift register. Once STT (bit 5 of register WR3) is set to a one, the uPD372 begins looking for the address mark pattern in the shift register. When the address mark pattern is found, a BRP (Bit Ring Pulse) is formed, the eight data bits in the shift register are transferred into the Read Register (RR2) and the Data Request flag is raised. From that point until STT is reset, every sixteenth bit clocked into the shift register causes a BRP and a Data Request and transfers the data bits to the Read Register.

Signals Required by the uPD372

In order to clock a bit into the uPD372 shift register, the desired logic level, zero or one, must be maintained at the READ DATA input (RD, pin 11) and a positive going transition must be made at the READ CLOCK input (RCK, pin 10).

The uPD372 samples RCK with the trailing edge of Ø2. Since RCK is asynchronous with Ø2, there is an uncertainty of one Ø2 clock cycle, Tcy, in the time when the uPD372 senses the positive going edge of RCK. Furthermore, RCK is not sampled instantaneously -- a setup time and hold time are required. Consequently, after RCK goes high, it must remain high for at least Tcy + 160ns to guarantee that the positive transition is

Data Conditioner Algorithm

The function of the DATA CONDITIONER is to translate the pulses of the raw data, read from a disk, into the RD and RCK signals required by the uPD372. Except for an amendment, which for the sake of clarity is introduced later, the DATA CONDITIONER performs the translation by using the following algorithm:

1. Each time a raw data pulse (clock or data) is received from a floppy disk drive, the DATA CONDITIONER sets the uPD372 RD input to a logic one and sends a positive pulse to the RCK input. The RD and RCK signals must meet the requirements of Figure 6. In addition, the receipt of a raw data pulse starts an interval timer

To meet this requirement the first sentence of the algorithm must be amended as follows:

1. Each time a raw data pulse (clock or data) is received from a floppy disk drive, the DATA CONDITIONER waits until the previous RCK cycle is completed and then sets the uPD372 RD input to a logic one and sends a positive pulse to the RCK input.

DATA CONDITIONER EXAMPLE

A DATA CONDITIONER which uses the above algorithm and with one-shot times set for IBM format is shown in Figure 9 along with a timing diagram. Tcy, the Ø2 cycle time, is assumed to be 5ØØns.

Raw data consisting of clock and data pulses is shown in the top line of the timing diagram. The first pulse occurs at time zero. The second pulse is missing indicating a logic zero. The third pulse is early by 6ØØns. The fourth pulse occurs at the expected time. This pattern is the worst case because of the short time interval between the decision that the second pulse is missing and the early third pulse.

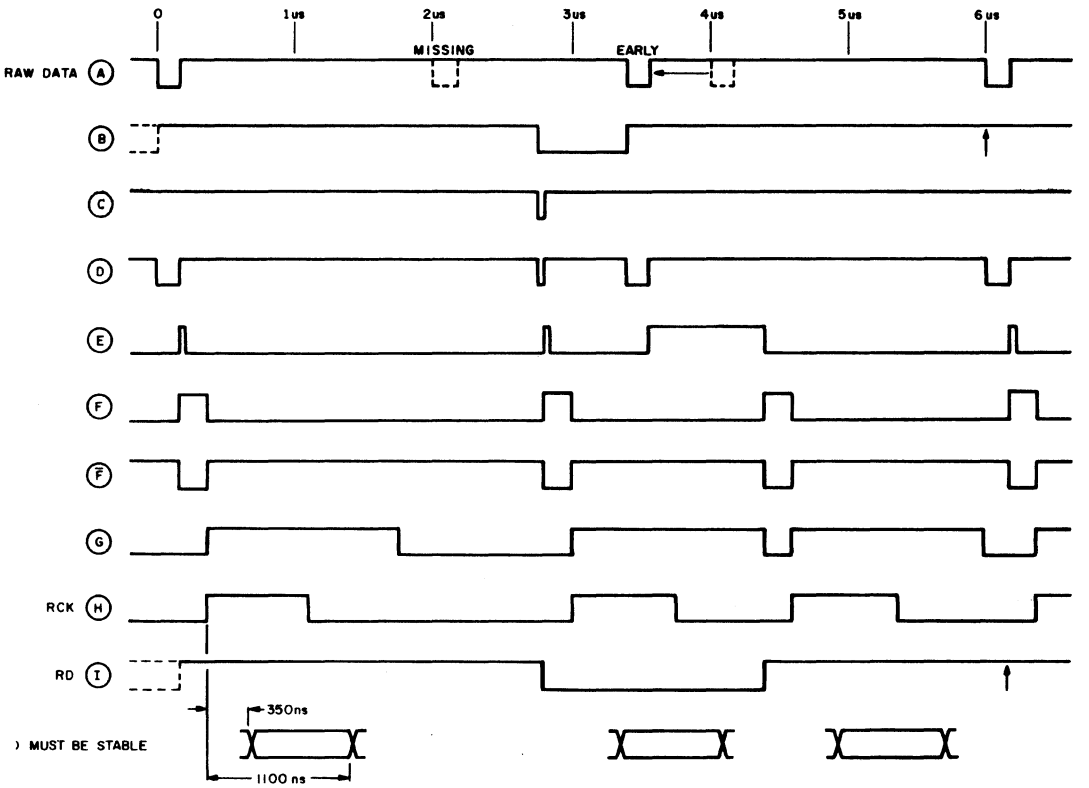
One-shot U31A generates the 1.4T time interval. Flip-flop U29A stores the information that a RCK cycle should begin when possible. One-shot U31B prevents the start of a RCK cycle until the previous cycle is completed. Flip-flop U29B double buffers the raw data. One-shot U30B forms RCK.

Other Formats and Other Ø2 Cycle Times

The same DATA CONDITIONER will operate with formats other than IBM and with Ø2 cycle times other than 5ØØns.

When using other formats the only parameter which affects the DATA CONDITIONER is the read data transfer rate and the only one-shot affected is the 1.4T time interval one-shot, U31A. The period of U31A should be 1.4T for all T. For example: T=2us in IBM Format so the period of U31A should be 2.8us and T=4us for the Shugart Minifloppy so the period of U31A should be 5.6us.

When using other Ø2 cycle times, the two one-shots which define RCK are affected. If the Ø2 cycle time is Tcy, then the period of U30B should be Tcy + 25Ø ns and the period of U31B should be 2 Tcy + 5ØØ ns in order to keep RCK consistent with Figure 6.



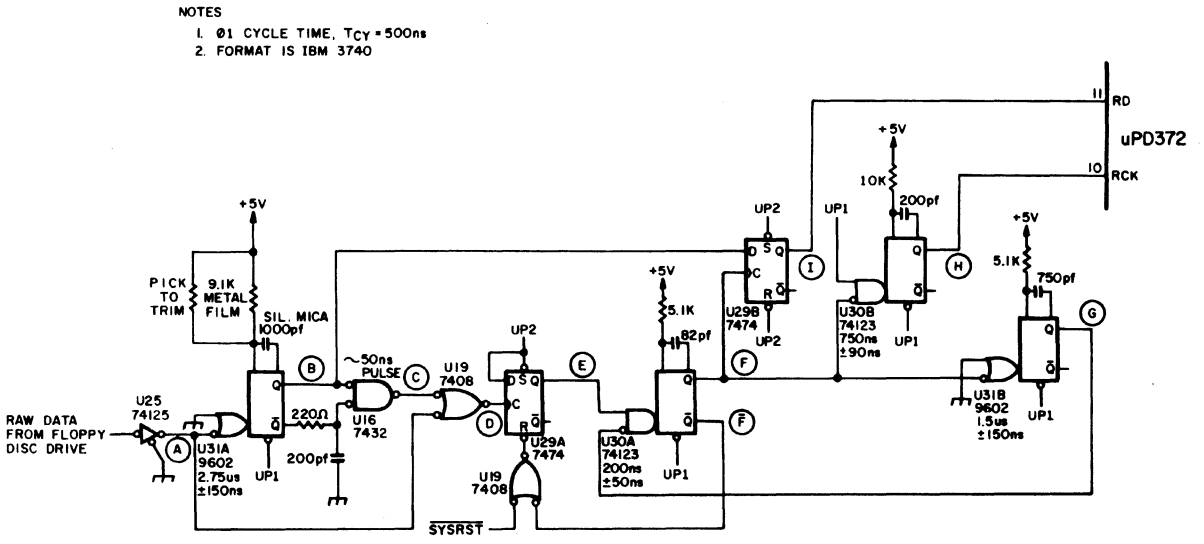


FIGURE 9
DATA CONDITIONER EXAMPLE AND TIMING DIAGRAM

FLOPPY DISK CONTROLLER EXAMPLE

HARDWARE

Figure 10 is divided into two sections. The section on the right shows a floppy disk controller which may be interfaced either directly to a host processor or indirectly through a controller processor. The section on the left shows a controller microprocessor system. Both the host and the controller processors are uPD8080A's in this example and the single floppy disk drive is IBM3740 compatible.

The controller and host processors share a common memory. 1K bytes of ROM is accessed by the controller processor between 0000-03FF of its address space. The same ROM is accessed by the host processor between E000-E3FF of its address space. 256 bytes of RAM is accessed by the controller processor between 0400-04FF of its address space. The same RAM is accessed by the host processor between E400-E4FF of its address space. The ROM stores the Disk Handling Routines and the RAM provides temporary storage for data, commands, status, etc.

The controller processor system configuration shown in Figure 10 is a testbed for software and hardware changes in the floppy disk interface. The intent is to give the host processor (which is assumed to have an editor and a console) the ability to monitor the performance of the controller processor and the rest of the floppy disk interface. Consequently, the direction of Direct Memory Access is from the host into the controller rather than vice versa and no provision is made to allow the controller to interrupt the host.

An interrupt feature would require the addition of only two chips. The resulting controller would be satisfactory for many applications although the host would have to transfer data between the common RAM and the desired storage locations. A circuit which allows Direct Memory Access from the controller into the host would require several logic changes resulting in a net gain of a few chips.

Circuit Description

The circuitry to the right of the uPD372 in Figure 10 contains the line drivers and receivers for the floppy disk drive. One shot U26B "stretches" the 60-100ns wide Write Data (WD) pulses into the width specified by the drive manufacturer.

The logic below the uPD372 is the Data Conditioner which is described in the DATA CONDITIONER section.